REMARKS

Initially, it is noted that the final rejection, in paragraph 2, refers to U.S. 2003/1088260. This reference is not of record in the present application. To the extent the citation is not a typographic error, the final rejection is improper and should be withdrawn.

In the office action mailed June 16, 2006, claim 1 was rejected based on Rajski, 2006/0041814. There, it was asserted that the claim limitation "adding at least two columns to a compactor matrix for each circuit output that can produce an online logic value at the same time" was supported by the Rajski published application at paragraphs 66-68.

In a response mailed September 13, 2006, it was pointed out that this is not a proper rejection because the cited paragraphs are only in the Rajski publication which is predated by the present pending application. The provisional application upon which Rajski relies did not include that material.

In an office action dated December 19, 2006, the Examiner indicated that he disagreed and that Rajski "is still considered as prior art for at least claim 16."

Moreover, it was suggested that paragraph 48 of Rajski was supported by the provisional application. But no explanation of how claim 1 was ever rejected has been provided to this date. In paragraph 3 of the final rejection, it is stated that the Rajski application is still considered as prior art because the rejection can be found in paragraph 64 of Rajski, which is supported by the provisional application at Section 1, introduction, paragraphs 4-5, Section 2, FSS compactor, 1st paragraph, and Section 7, experimental results, second paragraph. What exactly this material supports is never explained.

In Section 1, paragraphs 4 and 5 of the Rajski provisional application talk about an infinite response compaction scheme. Nothing therein talks about adding at least two columns to a compactor matrix for each circuit output that can produce an unknown logic value at the same time. There is absolutely no discussion of any such thing, and the one paragraph discussion of infinite input response compaction schemes. Paragraph 5 talks about a different type of compactor, a space compactor. There is no discussion of the claimed subject matter there either. There is a statement that it can handle unknown states and responses without circuit modification, but this is apparently relied previously with respect to claim 16. It has no apparent relation to claim 1. Also cited is section 2, FSS compactor, the first paragraph. However, there is no discussion of adding two columns of a compactor matrix that can produce an unknown logic value at the same time. It is unclear why this paragraph is being cited. There is no discussion of any

adding of any type. It is believed that this material was cited with reference to claim 16, but its application to claim 1 is unexplained and it is respectfully submitted, unexplainable.

Finally, section 7, experimental results, is cited, but, again, there is nothing whatsoever even mentioned about adding two columns of a compactor matrix for each circuit output that can produce an unknown logic value at the same time. In short, the rejection is not supported in any reasonable way. None of the claims dependent on claim 1 are even addressed. For this additional reason, a *prima facie* rejection of the dependent claims is not made out.

Claim 9 is never addressed, nor is any of its dependent claims. Therefore, a *prima facie* rejection is not made out.

Claim 16 calls for a plurality of exclusive OR gates arranged to handle any number of scan chains with unknown logic values. Again, taking each of the cited material, none of these talk about handling any number of scan chains. For example, page 1, fifth paragraph in connection with space compactors, says these types of devices can handle unknown states and responses without circuit modification. But this does not mean that it can handle any number of such unknown responses.

In the material relied on by the Examiner under the heading 2. FS Compactor, it is explained that no odd number of errors or two errors injected at the same time or in different time frames can mask each other completely. Also, single errors injected in each scan propagate to outputs in a different recognizable pattern. Thus, it is clear that Rajski's system cannot handle any number of scan chains with unknown values.

This is made even more clear on page 3 under the heading 3. Error Masking in the Absence of X States. There, it is explicitly stated that, as shown above, detection of errors in multiplicity 4 and higher even multiplicity is not guaranteed. In the ensuing section, Error Masking in the Presence of X States, it is explained that, because of the basic properties of polynomials, a single X state injected into the compactor, either at the same scan out cycle or another one, will not be able to mask entirely the error syndrome. Clearly, Rajski concedes that his compactor does not meet the claimed limitation.

Therefore, reconsideration is requested.

The assertion that Rajski's paragraph 5 indicates that any number of unknowns can be supported is incorrect. All that it says is that an unknown value can be supported, but not any value. Moreover, there is no teaching of any sort to explain how one or more unknown values could possibly be supported by the so-called space compactor, which is not even believed to be the subject matter of the Rajski article. Thus, even if it had said that any number could be supported,

it would fail to teach how to do it and, therefore, would be non-enabling and ineffective as prior art. See M.P.E.P. § 2121. Again, none of the claims dependent on claim 16 are even addressed, nor is claim 19 or any of its dependent claims.

Thus, it is respectfully submitted that a *prima facie* rejection is not made out and reconsideration would be necessary.

Respectfully submitted,

Date: April 25, 2007

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation